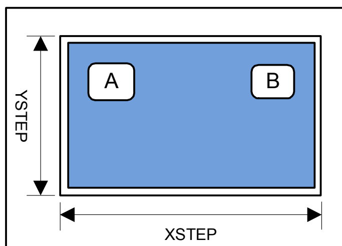
SmartCap Series Precision Thin-Film Capacitors

Features

- Ultra-low profile (0.18 mm height)
- Dual topside wirebonding pads
- Optional sputtered gold backside flow
- Superior breakdown voltage performance
- High quality LPCVD nitride dielectric
- Capacitances from 22 pF to 82 pF
- Tolerances down to ±2%
- 100% electrically tested
- Low effective series resistance (ESR)
- Topside passivation for pick and place handling
- Available as inked wafers or on wafer film frame
- RoHS compliant and Pb-free

Applications

- 13.56 MHz contactless smart cards
- RFID resonance circuits
- Chip-on-Board (COB) designs
- Known Good Die (KGD) programs
- IC downbond capacitors
- Embedded substrates



Description

The QuickSil SmartCap capacitors use a semiconductor wafer manufacturing process to create a low-profile thin-film capacitor with an extremely stable silicon nitride (Si_3N_4) dielectric. SmartCap capacitors are optimized for tuning applications including 13.56MHz ISO 15693 smart cards, ISO 18000-3 RFID item management tags, and other capacitor applications that require precision and high frequency operation in an ultra-thin profile.

QuickSil capacitors use LPCVD silicon nitride as the capacitor dielectric. LPCVD outperforms the plasma-enhanced (PECVD) dielectrics used by other thin-film manufacturers, yielding a film of superior uniformity and electrical breakdown characteristics. The result is a rugged capacitor which is better suited to the high transient voltages of RFID antenna coil applications.

Each capacitor has two topside wirebonding pads to support Chip-on-Board (COB) and Direct Chip Attachment (DCA) manufacturing flows. Electrode (A) is formed from semiconductor-grade aluminum. Electrode (B) is the heavily doped silicon substrate. Capacitor layout is optimized to minimize ESR. The result is a cost-effective capacitor with a high Q characteristic and excellent temperature stability. Optional backside gold metallization allows node (B) to be contacted through the backside substrate, allowing the use of a single topside bondwire to (A). The capacitors are passivated with an additional silicon nitride topside layer to protect the die during pick-and-place handling.

Custom capacitor layout, values, and tolerances are available as special orders. Please contact the factory at sales@quicksil.com.

QuickSil is an ISO 9001:2000 registered company.

Part Numbering

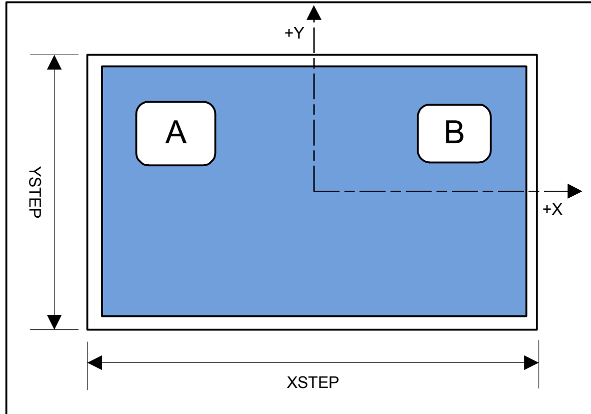
QSSC	S1	L	561	J	5W
Series	**Layout**	**Dielectric**	**Capacitance Code**	**Capacitance Tolerance**	**Packaging Code**
QSSC	S1 = bond pad layout	L= LPCVD silicon nitride dielectric	Capacitance expressed in pF using 3 digit format. Third digit indicates powers of 10. Example: 56pF = ‘561’	G = ±2% J = ±5% K = ±10%	5W = 125 mm wafer 5WG = 125 mm wafer with backside gold 5F = 125 mm scribed wafer on film frame 5FG = 125 mm scribed wafer on film frame with backside gold

Electrical Specifications[1]

Parameter	Symbol	Conditions
Capacitance	C	1 MHz, 1 V rms, 100% electrically tested
Temperature Coefficient of Capacitance	TCC	+45 ±25 ppm/°C
Operating Temperature Range	T_{OP}	-55°C to +125°C
Insulation Resistance	IR	> 10^{10} ohms
Aging	AR	No aging effect
Working Voltage	WV	Maximum continuous operating voltage
Breakdown Voltage	V_{BR}	> 1.5 X working voltage

Notes:
1) All measurements at 25°C unless otherwise specified.

Type S1 Capacitor Layout



Capacitance Ranges

Capacitance (pF)	Capacitance Code	Available Tolerances[2]	WV (volts)
22	221	G, J, K	30
27	271	G, J, K	30
33	331	G, J, K	30
39	391	G, J, K	30
47	471	G, J, K	30
56	561	G, J, K	30
68	681	G, J, K	30
82	821	G, J, K	30

Notes:
2) G = ±2%, J = ±5%, K = ±10%

Physical Dimensions

Parameter	Symbol	Dimension	Units
Capacitor Length (typical)[3]	L	0.85 / (0.0334)	mm / (inches)
Capacitor Width (typical)[3]	W	0.50 / (0.0197)	mm / (inches)
Capacitor Thickness	T	0.18 ±0.02 / (0.0071)	mm / (inches)
Die Stepping Distance on Wafer in X Direction	XSTEP	900.0	microns
Die Stepping Distance on Wafer in Y Direction	YSTEP	550.0	microns

Notes:
3) Final L, W dimensions depend on conditions and equipment used for wafer sawing. Values shown above reflect a 50 micron kerf.

Bond Pad Coordinates

Pad	Connection	Parameter	X	Y	Units
Pad A	First Electrode	Center of Bond Pad[4]	-276.0	119.0	microns
		Width of Passivation Opening	156.0	125.0	microns
Pad B	Second Electrode (Common to Substrate)	Center of Bond Pad[4]	281.0	119.0	microns
		Width of Passivation Opening	146.0	115.0	microns

Notes:
4) Pad locations are referenced to the center of the die. The +Y direction is away from the wafer flat.