

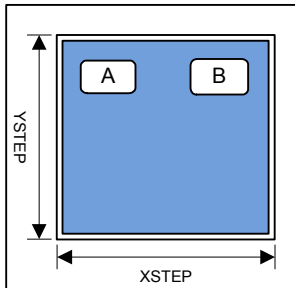
PolyCap Series Precision Thin-Film Capacitors

Features

- Ultra-low profile (0.18 mm height)
- Dual topside wirebonding pads
- Superior breakdown voltage performance
- High quality LPCVD nitride dielectric
- Capacitances from 220 pF to 820 pF
- Tolerances down to $\pm 2\%$
- 100% electrically tested
- Topside passivation for pick-and-place handling
- Available as inked wafers or on wafer film frame
- RoHS compliant and Pb-free

Applications

- 125 kHz clamshell proximity access cards
- 135 kHz RFID transponders
- Chip-on-Board (COB) designs
- Known Good Die (KGD) programs
- Embedded substrates



Description

The QuickSil PolyCap capacitors use a semiconductor wafer manufacturing process to achieve an extremely stable and low-profile thin-film capacitor based on a silicon nitride (Si_3N_4) dielectric. The capacitors are optimized for cost-sensitive applications where low profile and precision capacitance are required, such as 125 kHz security access card applications and RFID resonance circuits.

Each capacitor has two topside wirebonding sites to support Chip-on-Board (COB) and Direct Chip Attachment (DCA) manufacturing flows. The capacitor is comprised of a silicon nitride dielectric between a polysilicon lower electrode and an aluminum top electrode. This combination results in outstanding reliability and excellent stability over temperature.

An electrically isolated silicon substrate provides mechanical strength while allowing the use of either conductive or non-conductive die attach. The capacitors are passivated with an additional silicon nitride topside layer to protect the die during pick-and-place handling.

Custom capacitor layout, values, and tolerances are available as special orders. Please contact the factory at sales@Quicksil.com.

QuickSil is an ISO 9001:2000 registered company.

Part Numbering

QSPC	P1	L	682	J	5W
Series	Layout	Dielectric	Capacitance Code	Capacitance Tolerance	Packaging Code
QSPC	P1 = bond pad layout	L= LPCVD silicon nitride dielectric	Capacitance expressed in pF using 3 digit format. Third digit indicates powers of 10. Example: 680pF = '682'	G = $\pm 2\%$ J = $\pm 5\%$ K = $\pm 10\%$	5W = 125 mm wafer 5F = 125 mm scribed wafer on film frame

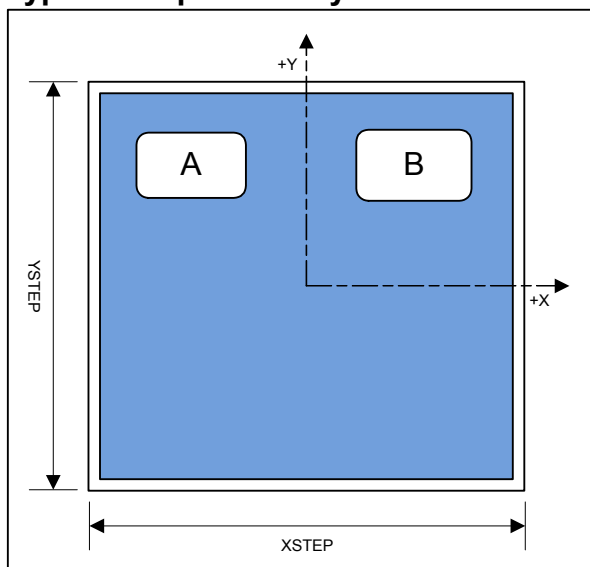
Electrical Specifications^[1]

Parameter	Symbol	Conditions
Capacitance	C	1 MHz, 1 V rms, 100% electrically tested
Temperature Coefficient of Capacitance	TCC	+45 \pm 25 ppm/ $^{\circ}$ C
Operating Temperature Range	T _{OP}	-55 $^{\circ}$ C to +125 $^{\circ}$ C
Insulation Resistance	IR	> 10 ¹⁰ ohms
Aging	AR	No aging effect
Working Voltage	WV	Maximum continuous operating voltage
Breakdown Voltage	V _{BR}	> 1.5 X Working Voltage

Notes:

- 1) All measurements at 25 $^{\circ}$ C unless otherwise specified.

Type P1 Capacitor Layout



Capacitance Ranges

Capacitance (pF)	Capacitance Code	Available Tolerances ^[2]	WV (volts)
220	222	G, J, K	75
270	272	G, J, K	60
330	332	G, J, K	50
390	392	G, J, K	40
470	472	G, J, K	35
560	562	G, J, K	30
680	682	G, J, K	25
820	822	G, J, K	20

Notes:

2) G = ±2%, J = ±5%, K = ±10%

Physical Dimensions

Parameter	Symbol	Dimension	Units
Capacitor Length (typical) ^[3]	L	0.94 / (0.0370)	mm / (inches)
Capacitor Width (typical) ^[3]	W	0.88 / (0.0346)	mm / (inches)
Capacitor Thickness	T	0.18 ±0.02 / (0.0071)	mm / (inches)
Die Stepping Distance on Wafer in X Direction	XSTEP	990.0	microns
Die Stepping Distance on Wafer in Y Direction	YSTEP	930.0	microns

Notes:

3) Final L, W dimensions depend on conditions and equipment used for wafer sawing. Values shown above reflect a 50 micron wide kerf.

Bond Pad Coordinates

Pad	Parameter	X	Y	Units
Pad A	Center of Bond Pad ^[4]	-262.0	275.0	microns
	Width of Passivation Opening	250.0	150.0	microns
Pad B	Center of Bond Pad ^[4]	242.0	275.0	microns
	Width of Passivation Opening	260.0	160.0	microns

Notes:

4) Pad locations referenced to the center of the die. The +Y direction is away from the wafer flat