

Bipolar Design and Layout Rules

<u>Reference</u>	<u>Description</u>	<u>7V</u>	<u>20V</u>	<u>40V</u>	<u>60V</u>
1.0	<u>Electrical Parameters</u>				
	Typical Parameters				
	HFE –NPN Transistor	70-250	80-300	80-300	70-240
	HFE –Lateral PNP Transistor (Note 1)	25-80	25-80	25-80	25-80
	HFE Substrate PNP Transistor		40-200	40-200	
	LVceo –NPN Transistor Minimum	8v	20v	40v	60v
	LVeco –Lateral PNP Transistor	10v	20v	40v	60v
	BVcbp –NPN Transistor Minimum	20v	40v	60v	110v
	BVebo –NPN Transistor	5.8- 6.7v	6.3- 7.0v	6.7- 7.5v	6.5-7.0v
	Vt –MOS Field Transistor (unimplanted)	10v	18v	35v	40v
	HFE Inverse I2L	>=1	>=1	>=1	>=1
	VCE (SAT) –NPN Transistor	<.35v	<.40v	<1.0v	<1.0v
	Schottky Forward Breakdown	.2-.45v	.2-.45v	.4-.7v	.4-.7v
	Schottky Reverse Breakdown	>8v	>20v	>40v	>60v
2.0	<u>Resistivities</u>				
	Substrate OHM*CM	6-15	4-12	4-12	7-15
	Buried Layer OHM/ []	15-30	15-30	15-30	15-30
	Epitaxial Layer OHM*CM	.3-.4	1.5-2.0	3.0-5.0	5.0-7.0
	Isolation OHM/ []	4.0-7.0	4.0-7.0	4.0-7.0	4.0-7.0
	Sinker OHM/ []		3.5-4.5	3.5-4.5	3.5-4.5
	Base OHM/ []	90-110	90-110	90-110	150+-15
	Emitter OHM/ []	2.9-3.5	2.9-3.5	2.9-3.5	2.9-3.5
	Aluminum mOHM/[]	20	20	20	20
	Note #1 lateral PNP HFE is dependent upon				
	Drawn P to P spacing				